REMARKS

I. Introduction

Claims 34-37, 39-48, 66, and 68-71 are pending in this application, of which claims 39 and 66 are independent. In this Amendment, claims 39-41, 66, 70, and 71 have been amended. Care has been exercised to avoid the introduction of new matter. Support for the amendment of claims 39 and 66 can be found in, for example, page 13, lines 8-11 of the specification and Fig. 1. Support for the amendment of claims 40, 70, and 71 can be found in, for example, Fig. 1 and relevant description of the specification. Support for the amendment of claim 41 can be found in, for example, Fig. 3 and relevant description of the specification.

II. Information Disclosure Statement

Applicants note that the Information Disclosure Statement filed December 21, 2006 has not been acknowledged. Applicants respectfully request the Examiner to clarify the record by acknowledging receipt of the IDS when reviewed and provide a copy of the PTO-1449 form appropriately initialed indicating consideration of the cited reference. An additional copy of the previously submitted PTO-1449 form is enclosed for the Examiner's convenience.

III. The Present Application

The present application describes a solid state imaging apparatus in which each of photoelectric conversion cells comprises a plurality of photoelectric sections (photodiode (PD) sections), configured to be able to share a floating diffusion (FD) section, a pixel amplifier transistor, and a read-out line.

For example, four photoelectric sections share one floating diffusion (PD) section, and two transfer transistors share one read-out line in each photoelectric conversion cell (see Fig. 1). In this case, there are a 0.25 floating diffusion section per PD section and a 0.5 read-out line per PD section (or transfer transistor).

Accordingly, the number of floating diffusion sections, pixel amplifier transistors, and read-out lines per PD section can be reduced in the solid state imaging apparatus. Therefore, it may be possible to increase an aperture ratio of the PD section (photoelectric element) to the photoelectric conversion cell (pixel), and downsize plane dimensions of the photoelectric conversion cell itself.

IV. The Rejection of Claims 34-37, 39-47, 68, and 70

Claims 34-37, 39-47, 68, and 70 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash. The Examiner asserted that Guidash, describing an active pixel image sensor, teaches the claimed subject matter.

Applicants submit that Guidash does not disclose or suggest a solid state imaging apparatus including all the limitations recited in independent claim 39. Specifically, Guidash does not teach, at a minimum, "in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines," as recited in independent claim 39.

In the Office Action, the Examiner, referring to Fig. 3b of Guidash, asserted that the reference teaches the claimed solid state imaging apparatus. Fig. 3b of Guidash illustrates pixel architecture 30 having four photodetectors (PD) 71-74 arranged in two rows and two columns;

transfer gates 51, 52, 61 and 62 for transferring charges from respective photodetectors 71-74; floating diffusion (FD) sections 41 and 42 connected to photodetectors 71-74 through transfer gates 51, 52, 61 and 62; and amplifier 32 connected to floating diffusion sections 41 and 42.

Applicants invite the Examiner's attention to terminals TG1b, TG1a, TG2b and TG2a connected to transfer gates 51, 52, 61 and 62, respectively, shown in Fig. 3b and a timing chart of Fig. 4 showing control pulses applied to the respective terminals. Fig. 4 shows that terminals TG1b, TG1a, TG2b and TG2a are respectively supplied with control pulses different from each other. Guidash teaches that there are four control signal lines connected to transfer gates 51, 52, 61 and 62, respectively, to provide the gates with different pulses, respectively. In other words, one control signal line (read-out line) is necessary for one photodetector (transfer gates) in Guidash.

In more detail, each photoelectric conversion cell (pixel) has four photoelectric sections (photodiodes) sharing substantially one floating diffusion (FD) section, and is provided with one control signal line (read-out line) per transfer gate in Guidash. Thus, there is one read-out line per photodiode section.

In contrast, claim 39 recites that a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines. For example, each photoelectric conversion cell has four photoelectric sections (PD sections) sharing one FD section, and two transfer transistors included in the same row or rows adjacent to each other share one read-out line in the each photoelectric conversion cell (see Figs. 1 and 3 of the present application). There is a 0.5 read-out line per photodiode section. Accordingly, it is possible to reduce wiring regions in one

pixel and thereby increase an opening area of the photodiode section with respect to one pixel. As a result, it can further possible to increase sensitivity of the solid state imaging apparatus.

Based on the foregoing, Applicants submit that Guidash does not disclose or suggest a solid state imaging apparatus including all the limitations recited in independent claim 39, within the meaning of 35 U.S.C. §103. Dependent claims 34-37, 40-47, 68, and 70 are also patentably distinguishable over Guidash at least because these claims respectively include all the limitations recited in independent claim 39. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

V. The Rejection of Claim 48

Claim 48 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash in view of Yamazaki et al. This rejection is respectfully traversed.

Claim 48 depends from independent claim 39. Applicants thus incorporate herein the arguments made in response to the rejection of claim 39 under 35 U.S.C. §103 for obviousness predicated upon Guidash. The Examiner's additional comments and secondary reference to Yamazaki et al. do not cure the deficiencies of Guidash. Yamazaki et al. simply discloses a display device in which a channel formation region in the semiconductor film is covered with the gate wiring, thereby shielding the channel formation region. Applicants, therefore, respectively solicit withdrawal of the claim and favorable consideration thereof.

VI. The Rejection of Claims 66, 69, and 71

Claims 66, 69, and 71 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Guidash and Patterson et al. The Examiner admitted that Guidash does not disclose that the

solid state imaging apparatus is part of a camera. However, the Examiner asserted that Patterson et al. teaches the missing feature of Guidash, and concluded that it would have been obvious to modify Guidash's device based on the teachings of Patterson et al. to arrive at the claimed invention.

Applicants submit that Guidash and Patterson et al., either individually or in combination, do not disclose or suggest a camera comprising a solid state image apparatus including all the limitations recited in independent claim 66. Specifically, the applied combination of Guidash and Patterson et al. does not teach, at a minimum, a solid state image apparatus "wherein in each photoelectric conversion cell, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines," as recited in claim 66. Claim 66 recites a camera comprising a solid state imaging apparatus similar to that recited in independent claim 39.

Applicants thus incorporate herein the arguments made in response to the rejection of claim 39 under 35 U.S.C. §103 for obviousness predicated upon Guidash. The Examiner's additional comments and secondary reference to Patterson et al. do not cure the deficiencies of Guidash. Patterson et al. simply teaches using a solid state imaging apparatus in electronic cameras. The reference does not teach that in a solid state imaging apparatus, a gate of a first transfer transistor included in the first row and a gate of a second transfer transistor included in the second row are connected to each other, sharing one of the plurality of read-out lines, as claimed. Dependent claims 69 and 71 are also patentably distinguishable over Guidash and Patterson et al. al least because these claims include all the limitations recited in independent claims 66.

Applicants, therefore, respectively solicit withdrawal of the rejection of claim 66, 69, and 71, and favorable consideration thereof.

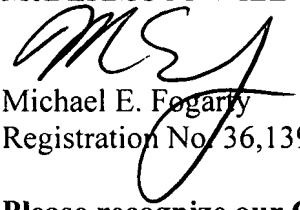
VII. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/lmm
Facsimile: 202.756.8087
Date: September 24, 2007

WDC99 1463704-1.060188.0710